RESEARCH ARTICLE

DESIGN, ANALYSIS AND SIMULATION OF CNTFET BASED SRAM CELLS.

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Manuscript Info

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Abstract

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This paper presents design, analysis and simulation of emerging memory device i.e. Static Random Access Memory (SRAM) cell. In nano-range devices, Carbon nanotubes field effect transistor (CNTFET) has shown a outstanding performance. CNTFET has been proved as better replacement for silicon devices. The characteristics of CNTFETs at different channel lengths and at different technologies are designed and analyzed. Complete current transport model is developed from carrier concentration in CNT for different chirality. The model describes the variation of charge developed on CNT with gate voltage. I-V characteristics have been efficiently modeled and compact model is developed for HSPICE circuit simulations. Finally 6T and 8T SRAM cell is designed with developed model and analysis is done for various performance metrics. Results show that CNTFET based 6T and 8T-SRAM consumes very less standby power with high static noise margins.

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Introduction:-
CMOS Technology in deep Sub Micron range seems to have reached saturation due to the increase in short channel effects and increased leakage current [1]. A promising alternative is CNTFET, which can overcome the limitations of Silicon based technology [2]. CNTFETs can have channel lengths of <10nm. Also, the Carbon nano tube interconnects have high strength and low resistance [3]. CNT transistors can help in scaling memory devices as they have very large current drives that depend on source & drain contact, the gate oxide and CNT diameter rather than the channel length [4]. So, we may go for much shorter channel lengths that help in physical scaling of the device. However, at channel lengths <10nm, quantum effects arise in CNTs [5]. SBCNTs cannot be substituted for CMOS login as SBCNTFETs convert their functionality from n-type to p-type and vice versa, depending on gate bias [3]. A CNTFET has very low OFF current, so power consumed is less.

Design Theory for CNTFET:-
The CNTFET is a 3 terminal device similar to a MOSFET. The silicon channel in the MOSFET is replaced with Carbon nanotubes in CNTFET. These CNTs are grown on a silicon substrate. The ends of these CNTs are doped with either n-type or p-type materials and the metal contacts are made over them. Materials such as Si_3N_4 are laid over the intrinsic CNT below the gate terminal that acts as the channel. The gate metal contact is made on the Dielectric (Si_3N_4). There is no restriction on the no. of CNTs in the device. A typical CNTFET device is shown in fig. 1.

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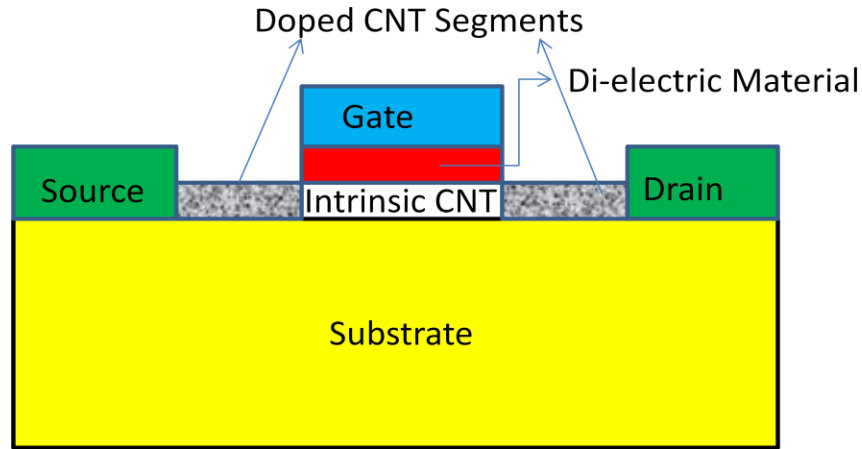Address:- Department Of ECE, K L University, Guntur, Andhra Pradesh, India.

Fig 1:- A typical CNTFET side view

In general CNTFETs are constructed using single walled Carbon nano tubes (SWCNTs). SWCNT consists of only one cylinder. A SWCNT is ambipolar. This means that it can act as either conductor or semiconductor based on the chirality vector, which is represented by (n, m). SWCNTs are used as channel in CNTFETs. The current in the channel (SWCNT) is dependent on the diameter of the tube, which in turn is dependant on chirality vector. The diameter of SWCNT can be given by the following equation.

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi} \sqrt{(n^2 + mn + m^2)}$$

----1

where a_0=0.142nm is the distance between two adjacent carbon atoms in the tube. The SWCNT acts as metallic when n=m or n-m=3i and as semi conductor otherwise.

In this paper the simulations are performed assuming the chirality vector (19,0). Also, the mobility of p-type and n-type carriers in CNTs are identical[6]. This makes the device symmetric in operation. This reduces the dynamic power dissipation in the circuit. Low leakage currents in CNTFETs reduce the static power dissipation.

Threshold voltages:-
The minimum voltage required to turn the transistor into 'ON' state is called Threshold voltage (V_t). The V_t of a CNTFET device can be given by the following equation.

$$V_t = \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{aV_\pi}{eD_{CNT}}$$

----2

Where:
a=2.49 ^{o}A is the distance between two adjacent carbon atoms in the tube.
V_π=3.033eV is Carbon π-π bond energy
D_{CNT} =CNTFET Diameter.

For a chirality vector (19,0) the D_{CNT} can be calculated from equation 1 as 1.49nm.
From equation 2, threshold voltage can be calculated from the defined parameters and is obtained as V_t=0.293V. The threshold voltage of CNTFET depends only on chirality of CNT. So, threshold voltage of CNTFET can be controlled by changing the diameter of CNT. For a given chirality, NCNTFETs have positive threshold voltage where as PCNTFETs have negative threshold voltage with same magnitude. The fig. 2 gives the variation of threshold voltage with change in chirality vector.
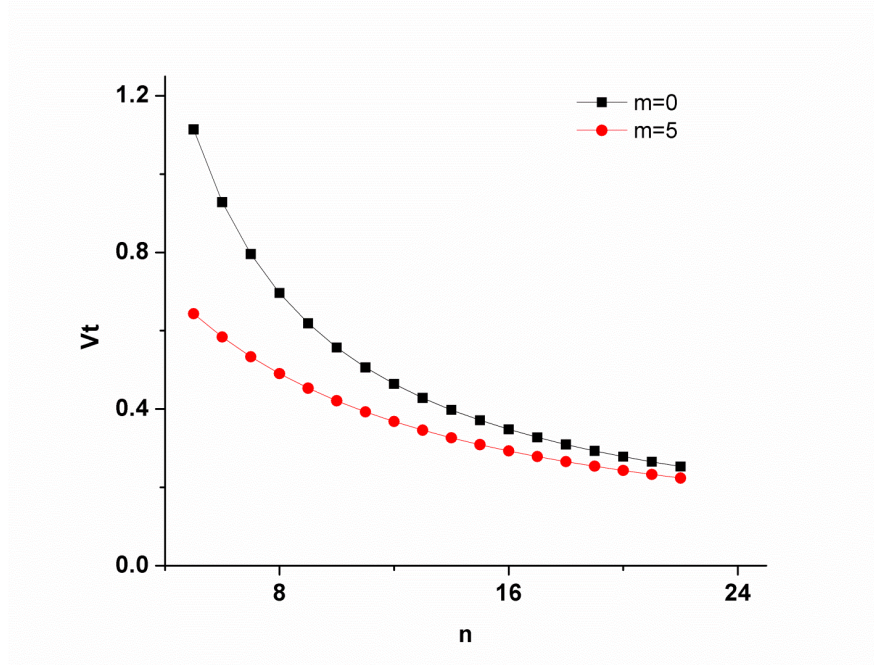
Fig 2: CNT chirality parameter n Vs. threshold voltage at chirality parameter m = 0 and 5

The increased interest in the area of CNTFETs is due to resemblance of their IV characteristics with that of a MOSFET. The IV characteristics are further discussed using simulation results. The current doesn't vary much with the increase in channel length, as in CNTFETs the current is dictated by the contacts rather than the channel length[4]. The current in the CNTFET is also dependant on the no. of tubes present in the device. So, it is very handy to increase the current density in CNTFETs than in the traditional MOS devices. The characteristics of CNTFET at different technology nodes, gate to source voltages are presented in the paper.

SRAM cell Design:-
SRAMs are very high-speed volatile memory devices used by embedded processors for transferring and storing of data. Due to low OFF currents and high-speed operation, CNTFETs can be substituted in SRAMs using CMOS and pass transistors logics. This greatly reduces the area and power consumption compared to CMOS SRAM at lower channel lengths.

A. **6T SRAM:-**
6T SRAM cell is the most used design in production of high-speed memory devices such as cache memory. The 6T SRAM cell is shown in the fig. 3.
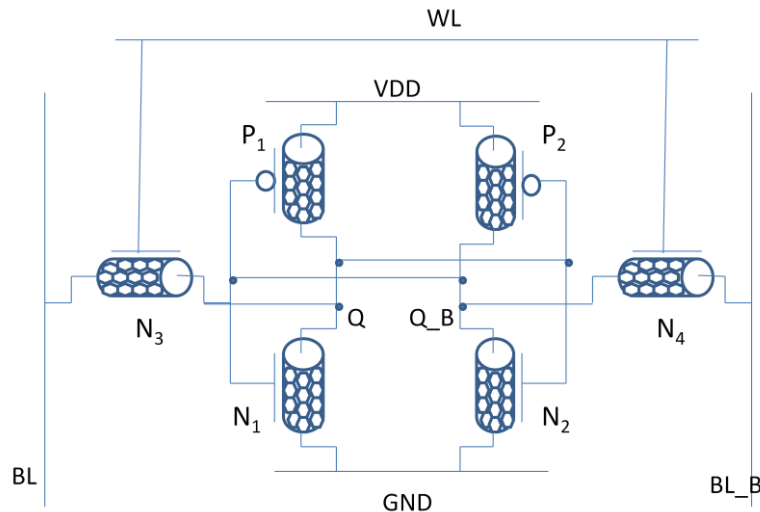
Fig 3: 6T CNTFET based SRAM cell

During write operation the bit lines BL and BL_B are driven with the necessary values to be stored. The word line (WL) is then turned ON. This drives the access transistors N_3 and N_4 into ON state thus feeding the BL and BL_B values to the cross-coupled Inverters. These value will be stored in Q and Q_B nodes. The data remains till the power supply goes OFF.

During read operation, BL and BL_B are pre-charged. When the WL is then turned ON the access transistors connect the Q and Q_B nodes to BL and BL_B lines. These bit lines will be pulled down to LOW depending on the values stored in Q and Q_B nodes.

8T SRAM:-
The bit line in the 6T SRAM cell get disturbed during read operation. 8T SRAM cell has an additional read port, which is completely isolated from the bit lines. The schematic of an 8T SRAM cell is as shown in the fig. 4. During write operation, the WBL and WBL_B are driven with necessary values. RBL and RWL have no effect during write operation and both are made LOW. During Read operation, the WWL is made LOW, RBL is pre-charged to HIGH and RWL is made HIGH. Depending on the voltage present at node Q_B, RBL discharges or remains at HIGH.
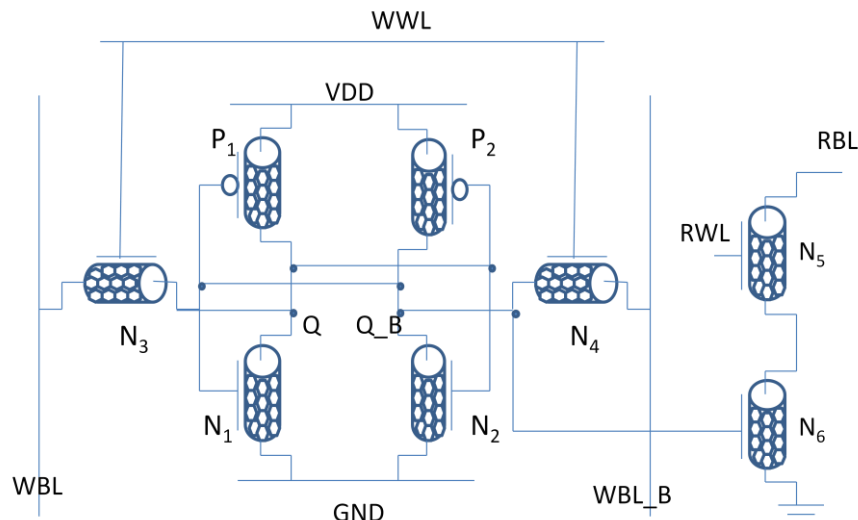

Fig 4:- 8T CNTFET based SRAM cell

The simulations are performed assuming the no. of tubes in inverter loop as 5 and in access transistors as 8.

Results and Discussion:-

The IV characteristics of a CNTFET at 32nm are shown in the fig. 5. The characteristics resemble that of a MOSFET. It is observed from the fig. 5 that the voltage required reaching the saturation level increases with the increase in channel length.
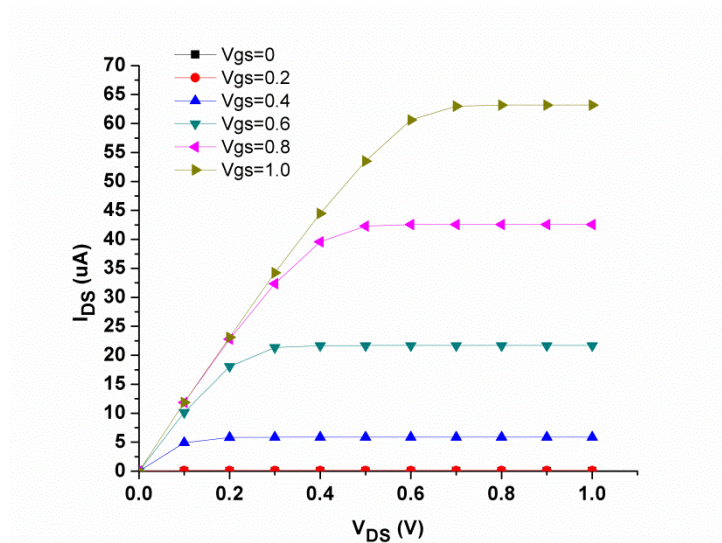

Fig 5:- I_{DS} Vs. V_{DS} of a CNTFET at channel length of 32nm and no. of tubes=1

The Fig. 6 represents the I-V characteristics of CNTFET at different channel lengths and at Gate to source voltage of 1.0 V. The simulation is performed assuming no. of tubes as 1.The current increases with increase in channel length. However, beyond 14nm the current doesn't vary much from one technology node to next technology node.
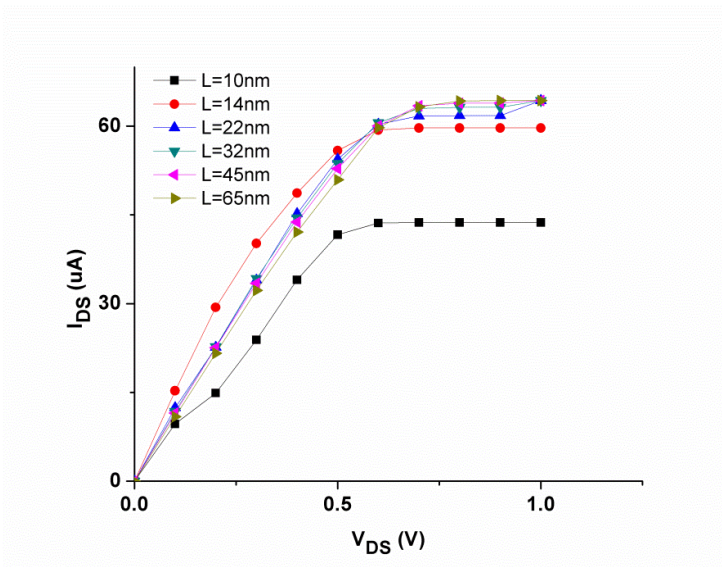

Fig 6:- I_{DS} vs V_{DS} at different channel lengths and V_{gs}=1.0 V

The Fig. 7 gives the variation of current with change in the no. of tubes present in device at 32nm and gate to source voltage of 1.0V. It is observed that the current in the channel increases with increase in the no. of tubes.
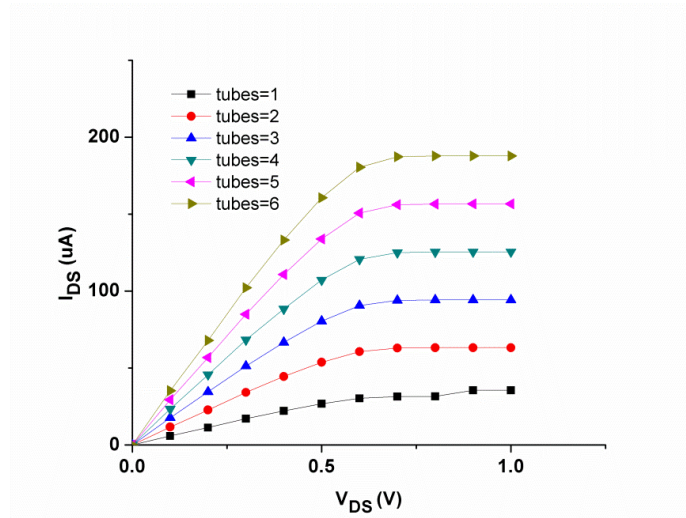
Fig 7:- Current variation with increase in the no. of tubes per device at channel length of 32nm.

Fig. 8 and Fig. 9 shows the variation of read and write delays of 6T and 8T SRAM cells at different supply voltages. It is clearly evident from the fig. 8 that the variation in read power in 6T and 8T SRAM cells is negligible at different supply voltages. The Read power remains almost same for 6T and 8T CNTFET based SRAM cells. However, during write operation 8T SRAM cell show better power than 6T SRAM cell.
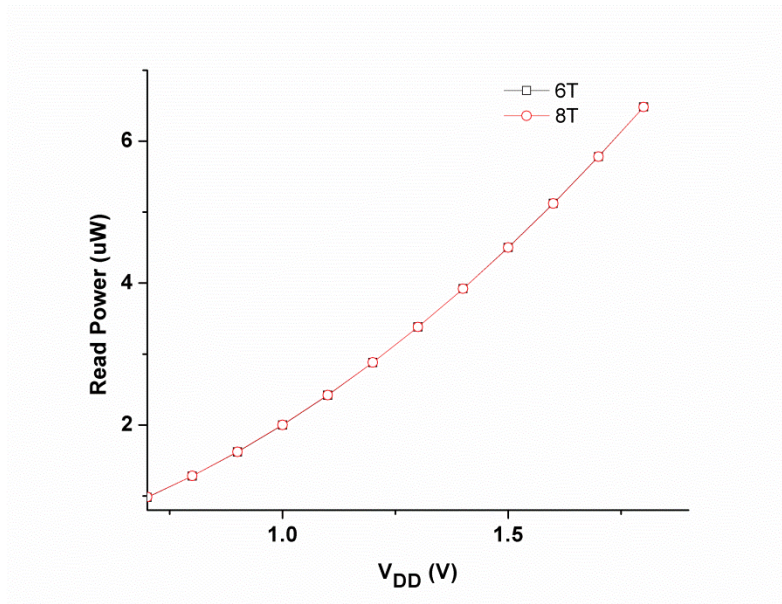

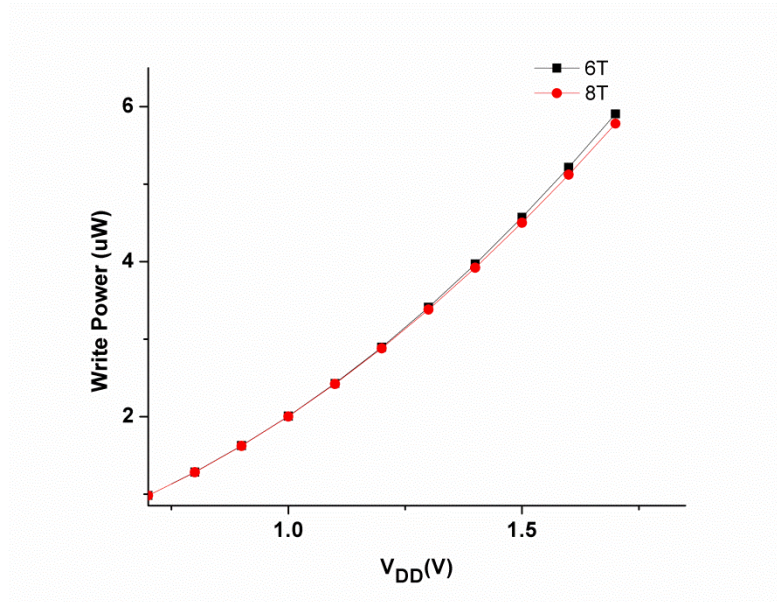**Fig 8:-** Read power Vs. V_{DD} for 6T and 8T SRAM cells

Fig 9:- Write power Vs. V_{DD} for 6T and 8T SRAM cells

The Read and write delays of both 6T and 8T SRAM cells vary with variation in supply voltage. Read delay of 6T SRAM cell is high compared to that of 8T cell.

The Read delay of 6T SRAM cell at different channel lengths by varying supply voltage is shown in fig. 10. At 14nm and 22nm the read delay is found to be varying with supply voltage. However, at 32nm the delay is constant from supply voltage of 0.9V onwards.
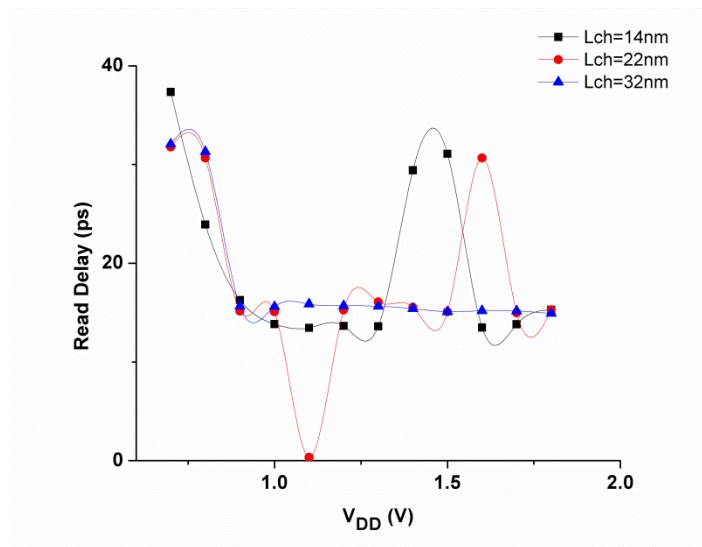

Fig 10:- Read delay of 6T SRAM cell at different channel length.

Fig. 11 shows the write delay of 6T SRAM cell at different channel length by varying supply voltage. At 14nm the write delay drops drastically at supply voltage of 1.0V and 1.7V. At 22nm and 32nm the write delay doesn't have any sudden variations.
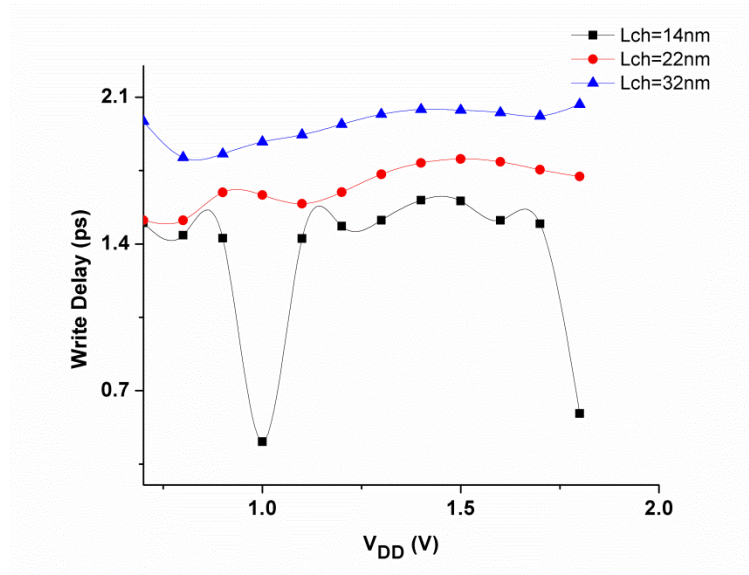
Fig 11:- Write delay of 6T SRAM cell at different channel length.

The Read delay of 8T SRAM cell at different channel lengths by varying supply voltage is shown in fig. 12. At 14nm, 22nm and 32nm the read delay is varying with supply voltage. The Read delay of 8T cell is constant at different supply voltages except at 1.4V.
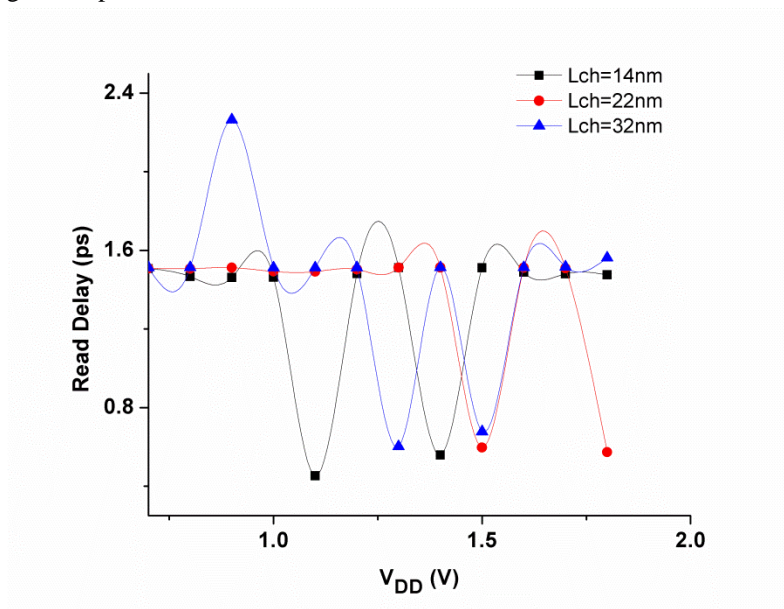

Fig 12:- Read delay of 8T SRAM cell at different channel length.

Fig. 13 shows the write delay of 8T SRAM cell at different channel lengths by varying supply voltage. At 14nm the write delay drops drastically at supply voltage of 1.2V and 1.6V. At 22nm and 32nm the write delay doesn't have any sudden variations. The write delay is almost constant at 32nm from a supply voltage of 0.9V.
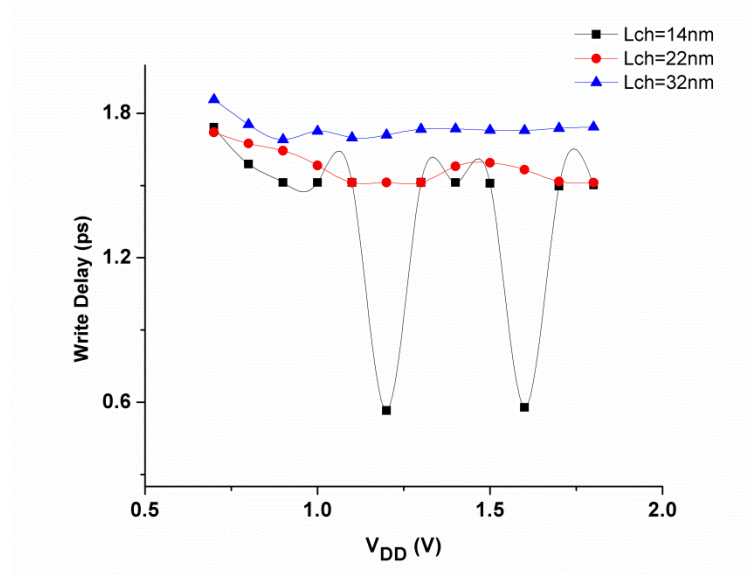
Fig 13:- Write Delay of 8T SRAM cell at different channel length.

Conclusion:-

The characteristics of the CNTFET are studied which prove that CNTFET is a better alternative to MOSFETs at deep submicron range. The characteristics of CNTFET are studied by varying different parameters like channel length, no. of tubes etc., A SRAM cell is designed replacing CMOS using CNTFETs in the conventional 6T cell design. The performance parameters like delay, average power has been presented. The write and read powers doesn't vary much at different technology nodes. From the analysis 32nm CNTFET based 8T SRAM cell has constant read and write delay at different supply voltages and at different technology nodes. Although the read and write delays are more at 32nm comparatively, they doesn't have any sudden changes and are almost constant throughout from a particular supply voltage of 0.9V except for read operation of 8T cell.

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